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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,154	09/08/2003	Mark L. Burgener	PER-005-PAP	5658

7590 12/12/2007

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EXAMINER	
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ART UNIT	PAPER NUMBER
2816	

MAIL DATE	DELIVERY MODE
12/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/658,154	BURGENER ET AL.	
	Examiner	Art Unit	
	Terry L. Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 September 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-71* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11,21,42 and 52* is/are allowed.

6)☐ Claim(s) *1-10,12-20,22-25,27-41,43-51,53-61 and 66-71* is/are rejected.

7)☒ Claim(s) *26 and 62-65* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 April 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

The amendment submitted on Sep 17, 2007 has been reviewed and considered with the following results:

Amended claims 46-47, 51, and 62 overcame their respective objection described on page 3 of the previous Office Action. Although those objections have now been withdrawn, amended claims 19 and 43 created new objections, and claim 19 also contains a previously overlooked objection. These claim objections are described later under the appropriate section.

After discussing the "cascaded sequentially" limitation in claim 1 with my supervisor, the phrasing is not considered acceptable since it is not clear how a single component can be cascaded. Therefore, the previous 35 U.S.C. 112 rejection of claim 1 remains, and is described later under the appropriate section with some minor modifications.

After reconsidering the applicants' comments, the question on page 4 of the previous Office Action that is related to a ring oscillator having a single section has been withdrawn. However, in its place, an objection to the drawings is described later since none of the figures clearly shows such a ring oscillator. For example, if the applicants' believe the references cited by the examiner should show everything, then it is also appropriate for the applicants to clearly show everything they claim (e.g. a ring oscillator with a single stage; or the plurality of switches connected in series).

Amended claim 19 overcame its rejection described on page 4 of the previous Office Action. Although that rejection has been withdrawn, the amended change created a new objection, which is described later under the appropriate section.

The applicants' explanation on page 15, with respect to "coupling substantial charge into the transfer capacitor via the charge pump clock input" as cited in claim 10 is not satisfactory, and has even made things more confusing to understand with respect to the claimed limitations. Although the applicants' own Fig. 7 does have substantial charge transferred via the charge pump clock input, how does that figure relate to the limitations recited within claim 1 as the applicants' comments imply? For example, how are the transfer capacitor coupling switches controlled in Fig. 7 so as to couple the transfer capacitor to a voltage source? Isn't that coupling done by the clock input itself, and not by one of the transfer capacitor coupling switches? Therefore, clarification is still requested with respect to claim 10, and this is described later under the appropriate section. Also, it is now requested that the applicants clearly identify which independent claims they believe that their Fig. 7 charge pump embodiment reads on. This will also help the examiner determine what the applicants are attempting to claim, and what might be considered allowable limitations.

The applicants' arguments/comments, with respect to "substantially sine-like", were not persuasive and have been maintained with respect to claims 12, 20, and 28. Those claim rejections are described later under the appropriate section, and related comments are described later under the Response to Arguments section.

Amended claims 13, 43, 60, and 62 overcame their respective rejections under 35 U.S.C. 112 as described on page 5 of the previous Office Action. Therefore, those rejections have been withdrawn. However, the amended section in claim 43 created a new objection, which is described later under the appropriate section.

Some of the amended claims overcame a few prior art rejections described in the previous Office Action. However, these are related to a change of claim dependency, and the addition of new claims. Since the amended claims, and the applicants' arguments/comments, did not clearly overcome the prior art rejections described in the previous Office Action, those rejections are described later under the appropriate section. However, some of the rejections have been modified to account for the newly added claims; change of claim dependency; and/or to further clarify the examiner's interpretation of the claimed limitations and the prior art reference(s) cited

Associated comments are described later under the Response to Arguments section.

Drawings

After considering the comments and what the applicants apparently believe should be clearly shown in the prior art references, the applicants' own drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, although Fig. 5 clearly shows a ring oscillator comprising three inverting driver sections cascaded sequentially, none of the figures shows a ring oscillator comprising only a single section (i.e. an odd number less than three). Therefore, a ring oscillator with only a single section must be shown or the feature(s) canceled from the claim(s) (e.g. see claims 1 and 43; and the implied one that falls under the "not more than three" cited in claim 40). Also, which figure(s) clearly show "more source switching devices disposed in series" and "more output switching devices disposed in series" as cited within both of claims 18 and 24, or the "more second-source switching devices disposed in series" and "more second-output switching devices disposed in series" as cited claim 19 since the "one or more" phrasing implies that more than one

devices is in series? As presently shown, only a single device is shown between the transfer capacitor and either the voltage source or the output voltage supply. Similarly, which figures shows the "more source switching devices disposed in series" as cited within claim 21? No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claims 19 and 43 are now objected to because of the following informalities: It is suggested "The apparatus of Claim 18, which...each recited feature" on lines 1-2 of claim 19's preamble be changed to --An apparatus comprising a charge pump as recited in claim 18,-- to minimize possible confusion with respect to what "each recited feature" refers to. Also in claim

19, it is suggested "stage" on line 2 be deleted unless claim 18 is amended to clearly identify a charge pump stage. This "stage" related objection had been previous overlooked (e.g. it had not been identified in the previous Office Action). Amended claim 43, line 8 "by by" should have one of the redundant terms deleted. Appropriate corrections are required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-10, 12-17, 20, 28-41, and 68 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicants regard as the invention. It is still not understood in claim 1 how an implied single inverting driver section (i.e. an odd number less than three) can be "sequentially cascaded", wherein "cascaded" implies a series of more than one component. Therefore, it is suggested the "sequentially cascaded" phrasing be removed from claim 1 and added to claim 68, which is understood to have three driver sections. Clarification is still requested with respect to what is meant by "coupling substantial charge into the transfer capacitor via the charge pump clock input" as cited in claim 10. For example, if Fig. 7 meets the limitations as the applicants imply, which transfer capacitor coupling switch(es) is controlled to couple the transfer capacitor to a voltage source as cited within claim 10's independent claim 1? The phrasing "substantially sine-like" in claims 12 (line 9), 20 (line 3), and 28 (line 10) is still considered relative, rendering the claims, and their corresponding dependent claims (if any), indefinite. The phrase is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, one of ordinary skill in the art would not be reasonably appraised of the scope of the

invention, and the applicants' present and previous comments have never clearly described what it actually means. For example, until the applicant clearly defines what is meant by "substantially sine-like", this examiner will still assume that any signal that is neither clearly shown nor described as a true square (or rectangular) wave that has sharp rising and falling edges (e.g. no, or at least minimal, transition times) will be considered "substantially sine-like"? These signals would include those that have at least one rising or falling edge that gradually changes in either a linear or non-linear manner (e.g. the transition between a logic high level and a logic low level is not substantially instantaneous). It is not clear what "an average voltage" relates to on lines 2-3 of claim 62.

Dependent claims carry over any rejection(s) from any claim(s) upon which they depend.

Claim Rejections - 35 USC § 103

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 18-19, and 49 remain rejected, and newly added claims 70-71 are rejected, under 35 U.S.C. 103(a) as being unpatentable over Imamiya, in view of Pfiffner, wherein both references were cited in the previous Office Action. Fig. 15B of Imamiya shows one type of a charge pump apparatus for generating output voltage supply at the common connection of C2 and QN12 of section 51-2, wherein section 51-1 of the apparatus comprises transfer capacitor C2; source switching device QN11 disposed between transfer capacitor C2 and voltage source VDD to convey transfer current from voltage source VDD when QN11 is conducting; output switching device QP12 is between transfer capacitor C2 and the output voltage supply at the common connection of C2 and QN12 of section 511-2 to transfer current from transfer capacitor C2 to the output voltage supply when QP12 is conducting; and it would have been obvious to one of ordinary skill in the art that a charge pump clock generating circuit (e.g. clock generator 902 shown in Fig. 2, wherein related oscillator 2 of Fig. 4 is disclosed as a ring oscillator for generating at least clock output Ø on column 4, lines 49-51) would be configured to generate single-phase charge pump clock output Ø coupled passively to the control node of source switching device QN11 of section 51-1 to cause conduction during charge periods (i.e. when Ø is high) and nonconduction during discharge periods (i.e. when Ø is low), and also to be coupled passively to the control node of output switching device QP12 of section 51-1 to cause nonconduction during charge periods (i.e. when Ø is high) and conduction during discharge periods (i.e. when Ø is low), wherein the charge periods will alternate with, and do not overlap, the discharge periods due to the known operation of PMOS and NMOS transistors receiving the same clock output Ø signal. Since clock output Ø is coupled to the gates of QN11 and QP12, no

substantial transfer current will be conveyed (i.e. MOS transistors are voltage controlled devices, and no substantial current will flow through their gate to their source or drain). Although clock output Ø is not specifically described as being passively coupled to the control nodes, it would have been obvious to one of ordinary skill in the art to consider the interconnecting line connecting the output of the charge pump clock generating circuit and the control nodes as one type of passive coupling. For example, the reference of Pfiffner discloses "passive elements are...interconnect lines" on column 1, lines 44-45. Therefore it would have been obvious to one of ordinary skill in the art to consider interconnect lines as one type of passive coupling that is without a distinct capacitor, resistor, or inductor type device. Thus, claim 18 is rendered obvious. Since each TC switching device of Imamiya is either an n-channel FET (i.e. see QN11-QN12) or a p-channel FET (i.e. see QP11-QP12), and nothing in Imamiya shows or discloses different thresholds among the same conductivity FETs, claim 70 is rendered obvious. Unless full voltage regulation and detecting are required, one of ordinary skill in the art would understand that the use of Fig. 2's R1, R2, CMP, 904, and 903 would not be necessary, and therefore the output of oscillator 902 would be applied to the input of charge pump 901 directly. The apparatus shown within Fig. 15B also shows second charge pump 51-2 comprising second transfer capacitor C2; second source switching device QN11 disposed between transfer capacitor C2 and voltage source VDD; and second output switching device QP12 disposed between transfer capacitor C2 and second output voltage supply OUT, wherein charge pump clock output Ø is coupled to both QN11 and QP12, wherein second source switching device QN11 of section 51-2 will conduct during charge periods (i.e. when Ø is high) and be nonconductive during discharge periods (i.e. when Ø is low), and second output switching device QP12 of section 51-2

will be nonconductive during charge periods (i.e. when Ø is high) and conductive during discharge periods (i.e. when Ø is low). This renders claim 19 obvious. In Fig. 15A, Imamiya's TC discharging switch QP11, under control of single phase charge pump clock output Ø, couples TC C2 to the output supply (e.g. the common connection between C2 and QN12 of section 51-2 during discharge periods (i.e. when Ø is low); and TC charging switch QN11, during charge periods (i.e. when Ø is high) that nonoverlappingly alternate with the discharge periods, and also under control of single-phase charge pump clock output Ø, couples TC C2 to voltage source VDD. Single-phase charge pump clock output Ø is passively coupled to the control node (e.g. gate) to TC discharging switch QP11 and TC charging switch QN11 because there is no intervening element between single phase charge pump clock Ø and Imamiya's control node, wherein an interconnecting line is considered as one known type of passive element as previously described. This interpretation of passive coupling renders claim 49 obvious. Method claim 71 is rendered obvious for the same type of reasoning as previously described with respect to claim 70.

Claims 1-4, 9-10, 12-14, 16-17, 28-33, 36-41, 43-45, and 48 remain rejected, and newly added claims 68 and 69 are rejected, under 35 U.S.C. 103(a) as being unpatentable over Imamiya, in view of Ito et al. (Ito), wherein both references were cited in the previous Office Action. Imamiya shows a charge pump apparatus in Fig. 15A that generates output voltage supply OUT (i.e. a voltage that is understood to be supplied to a subsequent section), wherein the charge pump apparatus comprises transfer capacitor C2, and a plurality of transfer capacitor coupling switches QN11-QN12,QP11-QP12, each switchable between a conducting state and a nonconducting state under control of at least charge pump clock output Ø. During periodic first

times (e.g. Ø is high), transfer capacitor C2 is coupled to voltage source VDD through transfer capacitor coupling switch QN11, and during periodic second times (e.g. Ø is low) that are not concurrent with the first times, transfer capacitor C2 is coupled to output voltage supply OUT through transfer capacitor coupling switch QP11. Although Fig. 15A does not clearly show a charge pump clock generating circuit, that provides charge pump clock output Ø, as a ring oscillator with an odd number of not more than three driver sections including circuitry to limit the rise and fall of each of the driver section's output, Imamiya does disclose the relationship between clock signals and an oscillator, such as a ring oscillator, for generating at least clock output Ø (e.g. see column 1, lines 36-37; and column 4, lines 49-51). Therefore, one of ordinary skill in the art would understand that charge pump clock output Ø, used to control the plurality of transfer capacitor coupling switches of Imamiya, would be provided by some type of a charge pump clock generating circuit, such as ring oscillator. Ito shows and discloses various examples of ring oscillators that provide a clock output. Therefore, it would have been obvious to one of ordinary skill in the art to utilize Ito's ring oscillator 70 (shown in Fig. 12) as the charge pump clock generating circuit/(ring) oscillator that provides charge pump clock output Ø to control Imamiya's plurality of transfer capacitor coupling switches. Ito's ring oscillator comprises three inverting driver sections (i.e. 59,51a,51b, 62;60,52a,52b,63; and 61,53a,53b,64) cascaded sequentially in a ring, wherein driver section 61,53a,53b,64 outputs charge pump clock output CLKO, which would correspond to Imamiya's charge pump clock output Ø. Each stage comprises circuitry to limit the rate of rise and fall of voltage at the driver section's output. For example, driver section 61,53a,53b,64 includes: 1) circuitry 61,53a configured as an active current limit to limit the rate of rise of voltage CLKO from a low level to a high level when 53a

is turned on, and circuitry 53b,64 configured as an active current limit to limit the rate of fall of voltage CLKO from a high level to a low level when 53b is turned on. This renders claim 1 obvious. The use of Ito's ring oscillator is just one example of a ring oscillator that would provide stable generation of charge pump clock output Ø (i.e. Ito's CLKO). Since Ito's ring oscillator has only three driver sections, claim 68 is rendered obvious. Each transfer capacitor coupling switch of Imamiya's Fig. 15A is controlled by charge pump clock output CLKO (of Ito) corresponds to Imamiya's Ø), and claim 2 is rendered obvious. Deeming the line coupling the clock output from Ito's charge pump clock generating circuit 70 to each of Imamiya's transfer capacitor coupling switches QN11-QN12, QP11-QP12 as one type of coupling circuitry, the signal will be coupled to each coupling switch without increasing the rise of voltage rise or fall, thus rendering claims 3-4 obvious. The current mirror configurations shown in Ito's Fig. 12, which limits source and sink currents conducted by each driver section, will ensure substantially identical magnitudes for limiting source and sink currents. For example, the sink currents through transistors 62-64 will correspond to the currents flowing within transistors 56-57, and the source currents through transistors 59-61 will correspond to the current flowing within transistor 58. With transistors 58 and 57 coupled in series between Vdd and Vss, their currents will be the same, and claim 9 is rendered obvious. Transfer capacitor C2 will be periodically coupled between voltage source VDD and ground in response to charge pump clock output Ø in order to charge, and a substantial charge will be coupled into transfer capacitor C2 through QN11 during those periods. With the conducting state of QN11 controlled by output Ø, the charge will be effectively via charge pump clock output Ø, thus rendering claim 10 obvious. In another interpretation of Imamiya's Fig. 15A, one of ordinary skill in the art would realize active

switches QN11 and QN12 allow transfer capacitor C2 to be charged, and active switches QP12 and QP11 allow transfer capacitor C2 to be discharged in an alternating, non-overlapping, manner. This would allow transfer capacitor C2 to be coupled alternately between source connection VDD and output connection OUT. Ito's Fig. 12 charge pump clock generating circuit 70 comprises active driver circuit 70 configured to source current (via 61,53a) to, and sink current (via 53b,64) from, charge pump clock output CLKO (of Ito, corresponding to Imamiya's Ø). The periodic switching of 61,53a and 53b,64 will effectively provide a waveform that is substantially sine-like (e.g. not a true square wave) due to the current limiting of 61 and 64, and capacitance 53c. Since clock output CLKO (Ø) will be coupled to the gates of Imamiya's MOS transistors QN11-QN12,QP11-QP12 (the plurality of active switches), there will be no substantial charge from clock output CLKO (Ø) that is coupled from source connections VDD to output connections OUT of transfer capacitor C2. Imamiya's circuitry 61,53a will limit the source current provided by active driver circuit 70 to clock output CLK0 (Ø), and circuitry 53b,64 will limit the current sunk from clock output CLKO (Ø), rendering claim 12 obvious. Discrete capacitive element 53c of Ito's charge pump clock generating circuit 70 is coupled to charge pump clock output CLKO, and this will help reduce voltage rates of change at that node, along with the current limiting previously described above, thus rendering obvious claim 13. Since charge pump clock generating circuit 70 includes a plurality of active driver circuits (e.g. 51a,51b; 52a,52b; and 53a,53b) configured to both source and sink current with respect to a corresponding driver output node, wherein circuitry 59-61 limits the current source capacity to each active driver circuit, and circuitry 62-64 limits current sink capacity in each active driver circuit, claim 14 is rendered obvious. Charge pump clock generating circuit 70 of Ito is one

known type of a current-starved ring oscillator due to 59-64, and claim 16 is rendered obvious. For the same type of reasoning as applied to claim 9 described above, claim 17 is also rendered obvious since the source current circuitry and sink current circuitry are configured to limit source and sink currents to a substantially identical magnitude. In another interpretation of the Imamiya/ Ito combination, Imamiya's discharging TCCS circuit QP11 couples transfer capacitor (TC) C2 to output supply OUT during discharge periods under control of first charge pump clock output CLKO (Ø) (i.e. when it is low); and Ito's 61,53a,53b,64 actively limit a rate of voltage change of the first charge pump clock output CLKO (Ø) during both positive and negative transitions such that a voltage of first charge pump clock output CLKO (Ø) is substantially sine like (e.g. not a true square wave), rendering claim 28 obvious. Imamiya's charging TCCS circuit QN11 couples transfer capacitor (TC) C2 to source voltage VDD during charge periods under control of second charge pump clock output CLKO (Ø) (i.e. when it is high) that nonoverlappingly alternate with the discharge periods (e.g. when one is high, the other is low); and Ito's 61,53a,53b,64 actively limit a rate of voltage change of the second charge pump clock output CLKO (Ø), and claim 29 is rendered obvious. Since the first/second charge pump clock outputs correspond to charge pump clock output CLKO (Ø), they are the same clock output, rendering claim 30 obvious. Also, all TCCS circuits QN11-QN12,QP11-QP12 are controlled by means of charge pump clock output CLKO (Ø), and they are all controlled by the first charge pump clock output, rendering claim 31 obvious. When TCCS circuit QN11 is conducting, TC C2 is connected to source voltage VDD during the charging period via charge pump clock output CLKO (Ø). Therefore, claim 32 is rendered obvious. Ito's current limiting circuit 61,53a,53b,64 limits current drive capacity of charge pump clock output CLKO/Ø, rendering obvious claim 33. Ito's first clock

generator driver circuit 61,53a,53b,64 is a driver circuit functionally incorporated in first clock generator circuit 70, which is configured to generate first charge pump clock output CLKO (Ø). First current limiting circuit 61,53a limits source currents from particular first clock generator driver circuit 61,53a,53b,64; and second current limiting circuit 53b,64 limits sink currents into the particular first clock generator driver circuit, rendering claim 36 obvious. Due to the current mirror relationships of 61 and 64 with 56-58, the source and sink currents will be limited to substantially identical magnitudes, and claim 37 is rendered obvious. First current limiting circuit 61,53a comprises current mirror device 61 (e.g. with respect to current mirror 58-61), and second current limiting circuit 53b,64 comprises different current mirror device 64 (e.g. with respect to current mirror 56-57,62-64), thus rendering obvious claim 38. Transistors 59-61 limit source currents, and transistors 62-64 limit sink currents, from all first clock generator driver circuits (e.g. 51a,51b; 52a,52b; and 53a,53b), and claim 39 is rendered obvious. Since Ito's first charge pump clock output CLKO/Ø is generated by means of current-starved ring oscillator 70, that includes three inverting driver sections 59,51a,51b,62; 60,52a,52b,63; and 61,53a,53b,64 coupled in a ring, claim 40 is also rendered obvious. When conducting and not in any transitioning phase, TCCS circuit QN11 couples TC C2 to source voltage VDD passively, and TCCS circuit QP11 couples TC C2 to output supply OUT. Therefore, under these conditions (i.e. conducting, and not transitioning), QN11 and QP11 will each be one type of a passive TCCS circuit, rendering claim 41 obvious. In another interpretation of the Imamiya/Ito combination, discharging switch circuit QP11 couples TC C2 to output supply OUT under control of first charge pump clock output CLKO (Ø) (i.e. when low); corresponding source current limiting circuits 59-61 limit source current provided to each corresponding driver output node within

current-starved ring oscillator 59,51a,51b,62/60,52a,52b,63/61,53a,53b,64 having three inverting driver stages (e.g. the first stage comprises 59,51a,51b,62); corresponding sink current limiting circuits 62-64 limit sink current drawn from each corresponding driver output node; and inverting driver output node CLKO of inverting driver stage 61,53a,53b,64 of the first charge pump clock generator is first charge pump clock output CLKO (Ø), rendering claims 43 and 69 obvious. TC C2 is coupled to source voltage VDD via charging switch circuit QN11, under control of second charge pump clock output CLKO (Ø) (i.e. when high), during charge periods alternating nonconcurrently with the discharge periods (e.g. only one of QN11 and QP11 is on at a time), and claim 44 is rendered obvious. Ito's capacitor 53c is coupled to driver output node CLKO of the first charge pump clock generating circuit to limit voltage transition rates of the driver output node, rendering claim 45 obvious. The connecting line between first charge pump output CLKO (Ø) and the control node (e.g. gate) of discharging switch circuit QP11 is one type of network (e.g. a network of a single line) that is not configured to increase rates of voltage change of the signal, and claim 48 is rendered obvious. [Note: The rates of voltage change are determined by the current limiting within 70.]

Claims 5-8, 15, 34-35, 46-47, 49, and 54-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imamiya/Ito as applied to their corresponding claim 68, 2, 12, 28 or 69 above, and further in view of Yamashiro, another reference cited in the previous Office Action. As previously described, the combination of Imamiya/Ito reads on the limitations recited within the basic claims. However, neither of those references clearly shows or discloses a capacitive coupling circuit configured to couple the charge pump clock output to a control node of at least one, or of each, transfer capacitor coupling switch. Fig. 1 of Yamashiro shows an example for

coupling one single input signal Vin to the control node of a pair of coupling switches Mn,Mp, and discloses these capacitors are for AC coupling and DC blocking with respect to sine like waves of an oscillating operation (e.g. see column 3, lines 9-12 and 55-66). Therefore, it would have been obvious to one of ordinary skill in the art to add a corresponding capacitive coupling circuit between clock output CLKO of Ito's charge pump clock generating circuit 70 (corresponding to clock output Ø of Imamiya's circuit) and the control node of each of the plurality of transfer capacitor coupling switches QN11-QN12,QP11-QP12 of Imamiya's circuit, rendering claims 5-6 obvious, wherein capacitive coupling is one known type of coupling circuitry. Use of coupling (or blocking) capacitors are well known to those of ordinary skill in the art, and these capacitive coupling circuits will block any unnecessary DC component from Ito's charge pump clock generating circuit 70, while still allowing the AC component of clock output CLKO (Ø) to control Imamiya's transfer capacitor coupling switches. This would minimize any inaccurate triggering of the coupling switches due to unwanted DC biasing. Since none of these capacitive coupling circuits would directly conduct substantial charge to transfer capacitor C2, claims 7-8 are also rendered obvious. For the same type of reasoning as applied to claims 5-6 above, claims 15, 34-35, and 46-47 are rendered obvious. However, it is noted that the transfer capacitor coupling switches of claims 5-6 are now identified as: 1) active switch(es) within claim 15; 2) TCCS circuits within claims 34-35; and 3) discharging (or charging) switches within claims 46-47. Also, the capacitive coupling switches of claims 5-6 are now identified as capacitive coupling networks within claim 15. The corresponding capacitive coupling circuit is one type of network that couples clock output CLKO (Ø) to the control nodes of the discharging switch circuit QP11, and it will not be configured to increase rates of voltage change of the

signal. Therefore, claim 48 is rendered obvious. The rate increase will actually depend on Ito's current limiting abilities. For the same type of reasoning previously presented above, claims 49 and 56-59 are also rendered obvious. Also, although Fig. 15A of Imamiya shows only a single stage for generating an output supply, Fig. 15B shows two stages 51-1 and 51-2, wherein one of ordinary skill in the art would understand section 51-1 closely corresponds to Fig. 15A with OUT and QP11 of Fig. 15A now corresponding to the common connection between C2 and QN12, and to QP12 coupled to that common connection. Therefore, one of ordinary skill in the art would also understand second TC C2 (of section 51-2) would be coupled to second voltage source VDD via second TC charging switch QN11 (of section 51-2) under control of clock output CLKO (Ø), and second TC C2 (of section 51-2) is coupled to second output supply OUT via second TC discharging switch QP11 (of section 51-2) that is also under control of clock output CLKO (Ø), rendering obvious claim 54. It would also have been obvious to one of ordinary skill in the art to couple clock output CLKO (Ø) to the control node of each TC charging switch, and each TC discharging switch, via corresponding capacitive coupling circuits as previously described above, rendering claim 55 obvious. The capacitive coupling circuit would provide AC coupling and DC blocking, thus helping to minimize false triggering of the switches due to inadvertent type DC biasing that would be coupled with clock output CLKO (Ø).

Claims 20 and 22-23 remain rejected under 35 U.S.C. 103(a) as being unpatentable over Imamiya/Pfiffner as applied to claim 18 above, and further in view of Ito et al. (Ito). As previously described, the combination of Imamiya/Pfiffner reads on the basic limitations recited within claim 18. However, the references do not clearly show or disclose circuitry for reducing voltage change rates of the charge pump clock output during both positive and negative

transitions. Similar to the reasoning described in some of the previous rejections above, it would have been obvious to one of ordinary skill in the art to utilize Ito's ring oscillator shown in Fig. 12 to provide clock output CLO as control signal Ø of Imamiya's circuit. With such a ring oscillator, circuitry 59-61 and 62-64 would reduce the voltage change rates of charge pump clock output CLKO (Ø) during both positive and negative transitions, wherein the clock output would be substantially sine-like. This renders claim 20 obvious. The use of Ito's ring oscillator, to provide clock output Ø to Imamiya's apparatus, provides one known type of charge pump clock generating circuit. For example, Ito's circuit is one specific type of a known clock generating circuit/ring oscillator, wherein Imamiya only shows/discloses the clock generator circuit/ring oscillator in generic ways (e.g. as oscillator 902 in Fig. 2 cited on lines 36-37 of column 1; and as clock generator 2 in Fig. 4 cited on lines 49-51 of column 4). Ito's circuit is one known means for providing a stable output clock. Ito's charge pump clock generating circuit 70 comprises circuitry 59-61 and 62-64 that limits current to each amplifying driver circuit (e.g. 51a,51b; 52a,52b; and 53a,53b) within charge pump clock generating circuit 70, and claim 22 is rendered obvious. Each of Ito's discrete capacitive devices 51c-53c 53c is coupled to a corresponding output of an amplifying driver circuit, thus limiting a rate of voltage change of that driver circuit's output. This renders claim 23 obvious.

Claims 50-51 and 53 remain rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Imamiya/Pfiffner as applied to claim 49 above, and further in view of Clark, another reference cited in the previous Office Action. As previously described, the obvious combination of Imamiya and Pfiffner reads on the limitations of claim 49. However, neither reference clearly shows or discloses the use of a plurality of TC discharging switches to couple

the TC to the output supply during discharge periods, or a plurality of TC charging switches to couple the TC to the voltage source during charge periods. Fig. 2 of Clark shows one example of a charge pump apparatus comprising a flying capacitor type circuit. Although Fig. 1 of Clark shows only single discharging switch 42 for coupling TC 30 to output supply 20b, and single charging switch 34 to couple TC 30 to voltage source 28, Clark also shows an example of using a plurality of TC discharging switches 42 (i.e. with two series coupled, unlabeled transistors), and a plurality of TC charging switches 34 (i.e. series coupled transistors 70 and 72) coupled to TC 30 in Fig. 2. Therefore, it would have been obvious to one of ordinary skill in the art to replace Imamiya's single discharging switch QP11 with a plurality of TC discharging switches controlled by clock output CLKO (Ø), as well as replace Imamiya's single charging switch QN11 with a plurality of TC charging switches also controlled by clock output CLKO (Ø), rendering claims 50-51 and 53 obvious. The plurality of series coupled charging switches, and series coupled discharging switches, would allow each switch within its plurality to drop less voltage across it, thus minimizing the possibility that a high voltage difference would cause any one switch to become damaged, and/not to operate effectively. For example, if only one switch (e.g. one single transistor) is used, the full amount would be dropped across it, while if two series coupled switches are used, the full amount would be divided between them, allowing each switch to have only half the full amount across each switch (e.g. assuming both switches are of the same size).

Claims 24-25, 27, 60-61, and 66-67 remain rejected under 35 U.S.C. 103(a) as being unpatentable over Imamiya in view of Yamashiro. Fig. 15A of Imamiya shows a charge pump apparatus for generating output voltage supply OUT, understood to be a voltage supplied to a

subsequent section. The charge pump apparatus comprises transfer capacitor C2 for conveying charge from voltage source VDD to output voltage supply OUT; at least one source switching device QN11 disposed between transfer capacitor C2 and voltage source VDD, and having a control node substantially isolated from both transfer capacitor C2 and voltage source VDD (e.g. the gate of QN11 is not coupled directly to either C2 or VDD); at least one output switching device QP11 disposed between transfer capacitor C2 and output voltage supply OUT, and having a control node substantially isolated from both C2 and OUT; and control nodes of the source/output switching devices QN11/QP11 receive charge pump clock output Ø. Although Imamiya does not show or disclose the use of a capacitive coupling circuit for coupling the clock output to the control nodes, one of ordinary skill in the art understands the use of a coupling/ blocking capacitor to provide AC coupling/DC blocking. For example, Fig. 1 of Yamashiro shows coupling one single input signal Vin to the control node of a pair of coupling switches Mn,Mp through capacitors C1,C2, respectively, and discloses these capacitors are for AC coupling and DC blocking with respect to sine like waves of an oscillating operation (e.g. see column 3, lines 9-12 and 55-66). Therefore, it would have been obvious to one of ordinary skill in the art to add a corresponding capacitive coupling circuit between whatever circuitry is providing clock output Ø to Imamiya's circuit and the control node of each of switching devices QN11,QP11, rendering claim 24 obvious. These capacitive coupling circuits would block any unwanted DC component from the charge pump clock output, while still allowing the AC component of clock output Ø to control the transfer capacitor coupling switches at the desired operating frequency. This would minimize any inaccurate triggering of the coupling switches due to unwanted DC biasing. The capacitive coupling circuit(s) would include a first capacitive

coupling circuit coupling clock output Ø to the control node of source switching device QN11, and a second capacitive coupling circuit coupling clock output Ø to the control node of output switching device QP11. Therefore, claim 25 is rendered obvious. Since source switching device QN11 (between C2 and VDD), and output switching device QP11 (between C2 and OUT) are each capacitively coupled to clock output Ø via their corresponding capacitive coupling circuit, claim 27 is rendered obvious. Interpreting the combination of Imamiya/Yamashiro in another manner, Yamashiro's first capacitive coupling network between clock output Ø and the control node of Imamiya's TC charging switch QN11 couples first charge pump clock output Ø to the control node and does not conduct a significant portion of the charge for output OUT, wherein TC C2 is coupled to source voltage VDD during charge periods via TC charging switch QN11 under control of first charge pump clock output Ø (i.e. when high); and Yamashiro's second capacitive coupling network between clock output Ø and the control node of TC discharging switch QP11 couples second charge pump clock output Ø to the control node and does not conduct a significant portion of the charge for output OUT, wherein TC C2 is coupled to output supply OUT during discharge periods, alternating nonconcurrently with the charge periods, via TC discharging switch QP11 under control of second charge pump clock output Ø (i.e. when low). This renders claim 60 obvious. Since second charge pump clock output Ø is first charge pump clock output Ø, claim 61 is also rendered obvious. When each actively controllable TC coupling switch QN11-QN12,QP11-12 of charge pump QN11-QN12,C2,QP11-QP12 is capacitively coupled to receive charge pump clock output Ø, claims 66-67 are rendered obvious. The capacitive coupling, as previously described above, would couple the AC components of clock output Ø to each of the control nodes, while blocking any unwanted DC components of the

clock output, thus minimizing inaccurate switching due to possible DC biasing associated with clock output Ø.

Claims 1-2, 4, 9-10, 12-14, 16-17, 28-33, 36-41, and 43-45 remain rejected, and new claims 68-69 are rejected, under 35 U.S.C. 103(a) as being unpatentable over Forbes et al. (Forbes), in view of Ito et al. (Ito), wherein both references were cited in the previous Office Action. Fig. 8 of Forbes shows a charge pump apparatus, for generating output voltage supply VOUT, comprising transfer capacitor 412; plurality of transfer capacitor coupling switches 488-492 coupled to transfer capacitor 412, wherein each switch is effectively switchable between conducting and nonconducting states under control of charge pump clock output Ø (e.g. either directly or indirectly).. During periodic first times (i.e. when Ø is high), switches 488-489 are conducting, while switches 491-492 are nonconducting, thus allowing transfer capacitor 412 to charge up by coupling it to voltage source 402. During periodic second times (i.e. when Ø is low) that is not concurrent with the first time, switches 488-489 are nonconducting, while switches 491-492 are conducting, thus coupling transfer capacitor 412 to output voltage supply VOUT. However, the reference does not show/disclose a charge pump clock generating circuit with a ring oscillator having three inverting driver sections; circuitry for limiting a rate of the voltage rise at a driver section output; or circuitry for limiting a rate of the voltage fall at the driver section output. Fig. 11 of Forbes shows a phase/waveform diagram for clock output Ø used within the Fig. 8 charge pump apparatus, and one of ordinary skill in the art would know numerous types of clock generating circuits are available for generating a single phase signal to effectively control the plurality of transfer capacitor coupling switches. Ito shows and discloses one such example in Fig. 12, wherein charge pump clock generating circuit 70 provides single

phase signal CLKO. Therefore, it would have been obvious to one of ordinary skill in the art to utilize Ito's charge pump clock generating circuit 70 to provide charge pump clock output CLKO as clock output Ø used to control Forbes' switches 488-492. Ito's charge pump clock generating circuit 70 includes a ring oscillator comprising three inverting driver sections (i.e. 59,51a,51b,62; 60,52a,52b,63; and 61,53a,53b,64) cascaded sequentially in a ring, wherein driver section 61,53a,53b,64 outputs charge pump clock output CLKO, which would effectively correspond to Forbes' charge pump clock output Ø. Each driver section comprises circuitry to limit the rate of rise and fall of voltage at the driver section's output. For example, driver section 61,53a,53b, 64 includes: 1) circuitry 61,53a configured as an active current limit to limit the rate of rise of voltage CLKO from a low level to a high level when 53a is turned on, and circuitry 53b,64 configured as an active current limit to limit the rate of fall of voltage CLKO from a high level to a low level when 53b is turned on. This renders claims 1 and 68 obvious. The use of Ito's ring oscillator is just one example of a charge pump clock generating circuit/ring oscillator that would provide stable generation of charge pump clock output Ø (i.e. Ito's CLKO). Since each transfer capacitor coupling switch is controlled by charge pump clock output Ø (e.g. switches 489 and 491 are controlled directly, while switches 488 and 492 are controlled indirectly), claim 2 is rendered obvious. Deeming the line coupling the clock output from Ito's charge pump clock generating circuit 70 to transfer capacitor coupling switches 489 and 491 as one type of coupling circuitry, the clock output will be coupled as a signal to at least one transfer capacitor coupling switch without increasing the rise of voltage rise or fall, thus rendering claim 4 obvious. The current mirror configurations shown in Ito's Fig. 12, which limits source and sink currents conducted by each driver section, will ensure substantially identical magnitudes. For example,

the sink currents through transistors 62-64 will correspond to the currents flowing within transistors 56-57, and the source currents through transistors 59-61 will correspond to the current flowing within transistor 58. With transistors 58 and 57 coupled in series between Vdd and Vss, their currents will be the same, and claim 9 is rendered obvious. Since transfer capacitor 412 will be periodically coupled between voltage source 402 and ground in response to charge pump clock output Ø in order to charge, a substantial charge will be coupled into transfer capacitor C2 through 489 during those periods, and with the conducting state of 489 being controlled by output Ø, the charge will be via charge pump clock output Ø, thus rendering claim 10 obvious. In another interpretation of Forbes' Fig. 8, one of ordinary skill in the art would consider switches 488-489 as active switches that allow transfer capacitor 412 to be charged when they are turned on, and switches 491-492 as active switches that allow transfer capacitor 412 to be discharged in an alternative, non-overlapping, manner. This would allow transfer capacitor 412 to be coupled alternately between source connection 402 and output connection VOUT. Ito's charge pump clock generating circuit 70 comprises active driver circuit 70 configured to source current (via 61,53a) to, and sink current (via 53b,64) from, charge pump clock output CLKO (of Ito, corresponding to Forbes' clock output Ø). The periodic switching of 488-489 and 491-492 will be provided by a waveform that is substantially sine-like (e.g. not a true square wave) due to the current limiting of Ito's 61 and 64, and capacitance 53c. Since clock output CLKO (Ø) will be coupled to the gates of Forbes' MOS transistors 489 and 491 (of the plurality of active switches), there will be no substantial charge from clock output CLKO (Ø) coupled from source connections 402 to output connections VOUT of transfer capacitor C2. Ito's circuitry 61,53a will limit the source current provided by active driver circuit 70 to clock output CLKO (Ø), and

circuitry 53b,64 will limit the current sunk from clock output CLKO (Ø), rendering claim 12 obvious. Discrete capacitive element 53c of Ito's charge pump clock generating circuit 70 is coupled to charge pump clock output CLKO, and will reduce voltage rates of change at that node, rendering obvious claim 13. Since Ito's charge pump clock generating circuit 70 includes a plurality of active driver circuits (e.g. 51a,51b; 52a,52b; and 53a,53b) configured to both source and sink current with respect to a corresponding driver output node, wherein circuitry 59-61 limits the current source capacity to each active driver circuit, and circuitry 62-64 limits current sink capacity in each active driver circuit, claim 14 is rendered obvious. Charge pump clock generating circuit 70 of Ito is one known type of a current-starved ring oscillator, and claim 16 is rendered obvious. For the same type of reasoning as applied to claim 9 described above, claim 17 is also rendered obvious since the source current circuitry and sink current circuitry are configured to limit source and sink currents to a substantially identical magnitude. With another interpretation of the Forbes/Ito combination, Forbes' discharging TCCS circuit 492 couples transfer capacitor (TC) 412 to output supply VOUT during discharge periods under control of first charge pump clock output CLKO (Ø) (i.e. when its low); and Ito's 61,53a,53b,64 actively limit a rate of voltage change of the first charge pump clock output CLKO (Ø) during both positive and negative transitions such that a voltage of first charge pump clock output CLKO (Ø) is substantially sine like (e.g. not a true square wave), rendering claim 28 obvious. Forbes' charging TCCS circuit 489 couples transfer capacitor 412 to source voltage 402 during charge periods under control of second charge pump clock output CLKO (Ø) (i.e. when its high) that nonoverlappingly alternate with the discharge periods (e.g. when 489 is off, 492 is on); and Ito's 61,53a,53b,64 actively limit a rate of voltage change of the second charge pump clock

output CLKO/Ø, and claim 29 is rendered obvious. Since the first/second charge pump clock outputs correspond to charge pump clock output CLKO/Ø, they are the same clock output, rendering claim 30 obvious. Also, all TCCS circuits 488-492 are effectively controlled by means of charge pump clock output CLKO (Ø), and they are thus all controlled by the first charge pump clock output, rendering claim 31 obvious. When TCCS circuit 489 is conducting, TC 412 is connected to source voltage 402 during the charging period via charge pump clock output CLKO (Ø). This renders claim 32 obvious. Ito's current limiting circuit 61,53a,53b,64 limits current drive capacity of charge pump clock output CLKO (Ø), rendering obvious claim 33. Ito's first clock generator driver circuit 61,53a,53b,64 is a driver circuit functionally incorporated in first clock generator circuit 70, which is configured to generate first charge pump clock output CLKO (Ø). First current limiting circuit 61,53a limits source currents from particular first clock generator driver circuit 61,53a,53b,64; and second current limiting circuit 53b,64 limits sink currents into the particular first clock generator driver circuit, rendering claim 36 obvious. Due to the current mirror relationships of 61 and 64 with 56-58, the source and sink currents will be limited to substantially identical magnitudes, and claim 37 is rendered obvious. First current limiting circuit 61,53a comprises current mirror device 61 (with respect to current mirror 58-61), and second current limiting circuit 53b,64 comprises different current mirror device 64 (with respect to current mirror 56-57,62-64), thus rendering obvious claim 38. Ito's 59-61 limit source currents, and 62-64 limit sink currents, from all first clock generator driver circuits (e.g. 59,51a,51b,62; 60,52a,52b,63; and 61,53a,53b, 64), and claim 39 is rendered obvious. Since Ito's first charge pump clock output is generated by means of current-starved ring oscillator 70, that includes three inverting driver sections 59,51a, 51b,62; 60,52a,52b,63; and 61,53a,53b, 64

coupled in a ring, claim 40 is also rendered obvious. When conducting and not in any transitioning phase, TCCS circuit 489 couples TC 412 to source voltage 402 passively, and TCCS circuit 492 couples TC C2 to output supply OUT. Therefore, under these conditions (i.e. conducting, and not in any transitioning phase), 489 and 492 will each be one type of a passive TCCS circuit, rendering claim 41 obvious. However, in another interpretation of what can be considered one type of a passive TCCS circuit, 492 does not directly receive clock output Ø. Therefore, it is one type of a passive TCCS circuit that will couple TC 412 to output supply VOUT due to its diode operating characteristics, but still being effectively controlled by clock output CLKO (Ø). This renders claim 41 obvious also. In another interpretation of the Forbes/Ito combination, discharging switch circuit 492 couples TC 412 to output supply VOUT under indirect control of first charge pump clock output CLKO/Ø (i.e. when low); corresponding source current limiting circuits 59-61 of Ito limit source current provided to its corresponding driver output node within current-starved ring oscillator 59,51a,51b,62/60,52a, 52b,63/61,53a, 53b,64 having three inverting driver stages 59,51a,51b,62; corresponding sink current limiting circuits 62-64 limit sink current drawn from its corresponding driver output node; and inverting driver output node CLKO of inverting driver stage 61,53a,53b,64 of the first charge pump clock generator is first charge pump clock output CLKO/Ø, rendering claim 43 obvious. TC 412 is coupled to source voltage 402 via charging switch circuit 489, under direct control of second charge pump clock output CLKO (Ø) (i.e. when high), during charge periods alternating nonconcurrently with the discharge periods (e.g. only 489 or 492 conducts at a time), and claim 44 is rendered obvious. Capacitor 53c is coupled to driver output node CLKO of the first charge

pump clock generating circuit to limit voltage transition rates of driver output node, rendering claim 45 obvious.

Claims 1-4, 10, 12, 14, 16, 43-44, 48, 50-51, 53, and 57-58 remain rejected, and newly added claims 68-69 are rejected, under 35 U.S.C. 103(a) as being unpatentable over Tasdighi et al., in view of Yamauchi, wherein both references were cited in the previous Office Action. Fig. 2 of Tasdighi shows a charge pump apparatus for generating output voltage supply Vout, wherein the apparatus comprises transfer capacitor C1; a plurality of transfer capacitor coupling switches SW1,SW2 with each switch switchable between conducting and nonconducting states under control of a charge pump clock output from charge pump clock generating circuit 24. Coupling switches SW1 and SW2 will each comprise CMOS inverter 26,27 shown in Fig. 3 (e.g. see column 3, lines 37-43), wherein each of transistors 26 and 27 is a distinct transfer capacitor coupling switch. One of ordinary skill in the art would understand the operation of Tasdighi's circuit, which is also described on column 3, lines 16-36. Transfer capacitor C1 charges when switches SW1,SW2 couple the upper terminal of C1 to voltage source Vin and its lower terminal to Gnd; and discharges when the switches couple the upper terminal to Gnd and its lower terminal to output voltage supply Vout. Therefore, one of ordinary skill in the art would know the transfer capacitor is alternately charged and discharged in accordance with the clock output provided by charge pump clock generating circuit 24. The charging would occur during periodic first times, and the discharging would occur during periodic second times that are not concurrent with the first times (e.g. both transistors 26 and 27 within its own respective switch SW1 or SW2 will not be full on, or off, at the same time). Although Tasdighi does not clearly show or disclose charge pump clock generating circuit 2 comprising a ring oscillator with no more than

three inverting driver sections, or circuitry for limiting current at a driver section's output, column 5, line 21 cites "Oscillator 14 could be a ring oscillator". Fig. 5 of Yamauchi shows/ discloses charge pump 37 receiving charge pump clock output CLK from charge pump clock generating circuit 39, which is clearly identified as a ring oscillator. Figs. 6 and 7 both show examples of this ring oscillator, wherein each figure shows it comprising at least three inverting driver sections. Therefore, one of ordinary skill in the art would understand Yamauchi provides support for the use of controlling a charge pump with a ring oscillator with an odd number of driver sections, which includes three sections. As such, it would have been obvious to one of ordinary skill in the art to use Yamauchi's ring oscillator 39 to provide its charge pump clock output CLK to the plurality of transfer capacitor coupling switches SW1,SW2 of Tasdighi. Using a version of three inverting driver sections from Yamauchi's Fig. 7, it has circuitry 49 configured as an active current limit to limit a rate of rise of voltage at each driver section's output, and circuitry 47 configured as an active current limit to limit a rate of fall of voltage at each driver section's output. Since the plurality of Tasdighi's transfer capacitor coupling switches will be under control of the particular charge pump clock output CLK (i.e. the output of the final driver section of the ring oscillator), claims 1-2 and 68 are rendered obvious. The use of a ring oscillator with only three driver sections requires fewer elements, takes up less area, and consumes less overall current, than a ring oscillator having a higher, odd number of driver sections. Deeming the line coupling the clock output from charge pump clock generating circuit (24 of Tasdighi; Fig. 7 of Yamauchi) to the control nodes of transistors 26,27 as coupling circuitry, the signal will be coupled to each coupling switch without increasing the rise of voltage rise or fall, thus rendering claims 3-4 obvious. Since transfer capacitor C1 will be periodically

coupled between voltage source Vin and Gnd in response to the charge pump clock output in order to charge, a substantial charge will be coupled into transfer capacitor C1 during those periods, rendering claim 10 obvious. One of ordinary skill in the art would realize switches SW1 and SW2 of Tasdighi allow transfer capacitor C1 to be charged and discharged in an alternative, non-overlapping, manner. Since a corresponding CMOS inverter of Tasdighi's Fig. 3 can be used for each active switch SW1,SW2, the apparatus of Tasdighi can be interpreted as comprising transfer capacitor C1; active switch 26 can be disposed in series between transfer capacitor C1 and voltage source Vin; active switch 27 can be disposed in series between transfer capacitor C1 and output voltage supply Vout; and charge pump clock generating circuit (of Yamauchi's Fig. 7) comprises active driver circuit 43,45 configured to source current (via 43) to, and sink current (via 45) from, charge pump clock output CLK. The periodic switching of 43 and 45 will provide a CLK waveform that is substantially sine-like. Since clock output CLK will be coupled to the gates of MOS transistors 26,27 (the active switches), there will be no substantial charge from the clock output coupled from the source connections to the output connections of transfer capacitor C1. Circuitry 49 will limit the source current provided by active driver circuit 43,47 to clock output CLK, and circuitry 47 will limit the current sunk from clock output CLK, rendering claim 12 obvious. Since Yamauchi's charge pump clock generating circuit comprises a plurality of active drivers (each comprising transistors 43 and 45), and circuitry 49/47 for limiting current sourcing/sinking capacities of each active driver circuit with respect to their corresponding driver output node, claim 14 is also rendered obvious. With circuitry 49 and 47, one of ordinary skill in the art would understand that the charge pump clock generating circuit of Yamauchi is configured as a current-starved ring oscillator, rendering claim 16 obvious. Using

only three driver stages within Yamauchi's first charge pump clock generator circuit as previously described above, and interpreting the Tasdighi/Yamauchi references in another manner, Tasdighi's transfer capacitor (TC) C1 is coupled to output supply Vout via a discharging switch (e.g. transistor 27 of Fig. 3, with respect to SW2 of Fig. 2); Yamauchi's corresponding source current-limiting circuit 49 limits the source current to each inverting driver output node of each driver stage 43,45; corresponding sink current-limiting circuit 47 limits the sink current drawn from each inverting driver output node; and the inverting driver output node of the last of the three inverting driver stages (of the first charge pump clock generator circuit) is first charge pump clock output CLK. This renders claims 43 and 69 obvious. Since TC C1 is coupled to source voltage Vin via a charging switch (e.g. transistor 26 of Fig. 3, with respect to SW1 of Fig. 2) controlled by second charge pump clock output CLK, during charge periods alternating nonconcurrently with the discharge periods, claim 44 is rendered obvious. The lines, going to the control nodes of the transistors 26 and 27 shown within Tasdighi's Fig. 3, are one type of network (e.g. each network comprising a single line), first charge pump output CLK is coupled as a signal to the control node of the discharging switch circuit, and claim 48 is rendered obvious. If one of transistors 26 and 27 of each of SW1 and SW2 is considered a discharge switch, and the other transistor is considered a charging switch, then there will effectively be a plurality of TC discharging switches, and a plurality of TC charging switches. For example, the charging switches would correspond to those switches coupling C1 between Vin and Gnd, allowing transfer capacitor C1 to charge, wherein the discharging switches would correspond to those switches coupling C1 between Gnd and Vout. Therefore, this plurality of discharging and charging switches render claims 50 and 51, as well as claim 53, obvious. Transistors 49 and 47

of Yamauchi make up circuitry that effectively reduces voltage change rates during both positive and negative transitions of charge pump clock output CLK since those elements reduce, or limit, the amount of current allowed to flow to the output node. Therefore, claim 57 is rendered obvious. Since Yamauchi's charge pump clock generator circuit (shown in Fig. 7) has at least one driver circuit (e.g. each set of transistors 43,45 can be considered a driver circuit), and transistors 49 and 47 limit the currents output from each driver circuit, claim 58 is rendered obvious.

Claim 49 remains rejected under 35 U.S.C. 103(a) as being unpatentable over Tasdighi/ Yamauchi in view of Pfiffner. Related to various rejections previously described above, one of ordinary skill in the art would understand that TC C1 would be coupled to output supply Vout during discharge periods via a TC discharging switch (e.g. 26 will conduct when clock output CLK/Ø is high); and coupling TC C1 to voltage source Vin via a TC charging switch (e.g. 27 will conduct when clock output CLK/Ø is low) during charge periods that nonoverlapplingly alternate with the discharge periods. Each of the switches is under control of single-phase charge pump clock output CLK/Ø. It would have been obvious to one of ordinary skill in the art that single-phase charge pump clock output CLK/Ø is passively coupled (e.g. coupled by an interconnecting line with no intervening elements) to the control nodes of the charging/ discharging switches (e.g. see Tasdighi's transistors 26,27 shown in Fig. 3, with respect to SW1,SW2 shown in Fig. 2), and the gate of each MOS transistor will substantially isolate transfer capacitor (TC) C1 of Tasdighi from Yamauchi's clock output CLK. Therefore, claim 49 is rendered obvious. For example, Pfiffner discloses that "passive elements are...interconnect

lines" on column 1, lines 44-45. Therefore, one of ordinary skill in the art would understand passive coupling does not require any distinct capacitor, resistor, or inductor type elements.

Claims 50-51 and 53 remain rejected under 35 U.S.C. 103(a) as being unpatentable over Imamiya/Ito/Yamashiro as applied to claim 49 above, and further in view of Clark. Applying the same type of reasoning as previously described above with respect to the rejections of claims 50-51 and 53 using only the Imamiya, Ito, and Clark references, claims 50-51 and 53 are again rendered obvious. The plurality of discharging switches and plurality of TC charging switches will provide a means for sharing the voltage drop across the switches within their respective plurality.

Allowable Subject Matter

Claims 11, 21, 42, and 52 are allowed. There is no motivation to modify or combine any prior art reference(s) to ensure: 1) the second control node AC impedance is at least twice the first control node AC impedance as recited within claim 11; 2) the second device area is greater than double the first device area as recited within claim 21; 3) the discharge output TCCS has a control node AC impedance at least double the control node AC impedance of the discharge common TCCS as recited within claim 42; and 4) the second TC discharging switch has a control node AC impedance at least twice as large as a control node AC impedance of the first discharging switch as recited within claim 52 .

Claims 26 and 62-65 are only objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. There is no motivation to modify or combine any prior art reference(s) to ensure: 1) the capacitive coupling circuit includes biasing circuitry that allows

an average control voltage to cause a switching device to be substantially nonconductive as recited within claim 26; or 2) the biasing is at an average of the time-varying voltage as recited within claim 62, upon which claims 63-65 depend.

Response to Argument

The arguments/comments within the amendment submitted on Sep 17, 2007 were reviewed and considered with the following results:

The applicant's arguments with respect to "cascaded sequentially" and "substantially sine-like" were fully considered but they are not persuasive. When elements are cascaded, there needs to be at least two of them. For example, one of ordinary skill in the art would not consider a single section within a ring oscillator as being cascaded with itself. With respect to the "substantially sine-like" related rejections, the invocation of an argument based estoppel does not relieve the applicants of the requirement under 35 U.S.C. 112, second paragraph to particularly point out and distinctly claim the subject matter of their invention. Although "substantially" is an acceptable term, and the applicants insist waveforms of prior art charge pumps are "not substantially sine-like", since the specification never provides sufficient guidelines as what constitutes a "substantially sine-like" signal, those rejections have been maintained. Related to this, it is not understood how the term "like" limits the claimed waveform. For example, of the numerous examiners this examiner has consulted, none of them can explain what is considered "substantially sine-like." Therefore, where is the evidence that "most persons of skill in the art readily understand the meaning of "substantially sine-like"" as cited on page 16 of the amendment? For example, it is not understood how the applicants' "substantially sine-like" covers a range of variation around a precise sine wave, yet limits coverage to waveforms that are

substantially like a sine wave. Thus, this argument does not provide evidence that clearly indicates how much variation is necessary to identify a waveform as being "substantially sine-like." Similarly, the applicants indicate that Forbes' reference shows trapezoidal waveforms that are "clearly not substantially sine-like" on page 27 of the amendment. However, not knowing what is clearly sine-like from the original disclosure, a trapezoidal waveform is considered one type of a substantially sine-like signal, wherein it alternates between peak high and low levels without having instantaneous (e.g. sharp, immediate) transitions. Even if a reference cited by the examiner cites pulse, pulse train, or clock, it is not known how this differs from the applicants' own CLK provided by the applicants' ring oscillator 500 shown in Fig. 5. For example, doesn't CLK (or clock) actually imply something other than a "sine-like" signal? The applicants' "CLK 524 may oscillate substantially rail-to-rail (e.g. between 0 to Vin+) with low dv/dt transitions, and may have a significantly sine-like shape" in paragraph 050 of page 12 of the original disclosure does not provide strong support to what is to be considered "sine-like." Since the applicants admit the CLK output 524 has low dv/dt transitions, and one of ordinary skill in the art understands that trapezoidal waveforms have low dv/dt type transitions, why can't trapezoidal waveforms also be considered "sine-like"? Therefore, it is not understood why the applicants require all references cited by the examiner to clearly show and disclose everything, while apparently ignoring the obviousness of the various modifications that one of ordinary skill in the art would understand as previously described above. If the examiner applied that type of reasoning to the applicants' own application, numerous areas are quite generic and clearly do not show/disclose everything in detail (e.g. ring oscillator with only a single stage; a sine-like signal; and series connected switching devices).

Although this examiner will agree with the applicants' comments that charge pumps are in a "crowded field", this examiner strongly believes the applicants are narrowly interpreting what is actually considered a charge pump, and that the applicants insist their claimed limitations relate only to the charge pump itself. This examiner, and all of those (of ordinary skill in the art) that have been consulted over the prosecution of this application, understand there is a strong distinction between what is typically considered a charge pump, and what provides at least one control signal, or how at least one control signal is provided, to the charge pump. Numerous prior art references show a charge pump (with either generic type switches or transistors used as switches) without any control signal(s) being supplied; some show lines indicating some type of control signal(s) is(are) provided, but does not show what actually provides the control signal(s); and some show a generic type signal generator that provides at least one clock signal to the charge pump. In these references, the descriptions indicate how a capacitor is charged, and then transfers its charge to provide a pumped (e.g. boosted) output voltage. The basic operation of a charge pump is well known to one of ordinary skill in the art, wherein the operation generally comprises two basic states. In one state, a capacitor is charged, and in another state, the capacitor's charge is transferred to an output as a pumped voltage. These basic operations are performed in an alternating sequence, wherein the capacitor is not allowed to charge and transfer charge at the same time. Known examples of these prior art references includes circuitry similar to some of the applicants' own figures. For example, the applicants' own Fig. 2 shows four basic switches S1-S4 in a generic fashion (the switches are neither shown as transistors, nor receiving any type of control signal), and Fig. 3 clearly shows four switches 304,306,312,314 as transistors each receiving a corresponding control signal from generic clock generator 350. However, from

the applicants' comments, the control of the switches, and what provides the control signal(s), is actually considered part of the charge pump itself, but this in only the applicants' interpretation. As previously stated above, the charge pump, and what provides its control, are typically understood as being two distinct sections by one of ordinary skill in the art. In fact, the applicants' even disclose "Innumerable alternative embodiments of the charge pumps described above are possible. Any clock generator may be employed....Any of these desirable features may be affected independently, or in combination with any of the other desirable features, or in combination with any other feature described herein. Thus, the skilled person may apply aspects of the method and apparatus described herein to a staggering variety of charge pump configurations" on page 18 of the original disclose.

Related to the applicants' disclosure that innumerable embodiments are possible and the skilled person may apply a staggering variety of configurations, page 18 of the amendment cites "evidence of an over-zealous effort to try to cobble together an argument for obviousness using improper hindsight." However, from this examiner's perspective, the applicants appear to over-zealously ignore all other references and knowledge of one of ordinary skill in the art, and then turn around and believe everything they disclose is novel, and that all types of variations of the applicants' own disclosure and figures, are acceptable. This is highly unreasonable, and it is not understood why the applicants' continue to insist that various obvious means for supplying at least one control signal to the charge pump is novel (e.g. by a ring oscillator such as one with only three stages or current starved/limited), and that this control is not obvious to one of ordinary skill in the art. Numerous references of record cited by the examiner have clearly shown charge pumps controlled by ring oscillators, including some that show (or at least

disclose) ring oscillators as having three stages, and/or current limiting. Therefore, is the perceived over-zealousness of the examiner basically a result of the applicants' own over-zealousness of not admitting to obvious type modifications with respect to what one of ordinary skill in the art understand when applying the broadest reasonable interpretation of the claimed limitations and prior art references?

Note: The examiner has identified (in this Office Action, and in previous Office Actions) allowable material, with respect to limitations restricted to the charge pump structure itself (e.g. claims 11, 42, and 52 have differences in AC impedances; claim 21 has devices of different areas; and claims 26 and 62 have biasing circuitry for a switching device.

To help resolve the numerous disagreements between the examiner and the applicants, the examiner requests the applicants to clearly indicate what is considered the novel, critical feature(s) of the present invention. For example, is it the use of: 1) a ring oscillator with no more than three stages; 2) a current starved ring oscillator; 3) current limiting; 4) single phase control; 5) a substantially sine-like clock output; 6) passive coupling; 7) capacitive coupling; 8) biasing; 9) differences in device areas; and/or 10) differences in AC impedance? Once this examiner understands that the applicants are seriously attempting to concentrate on actual novel type modifications, then prosecution of the application can be moved along swiftly. Otherwise, the numerous claims, embodiments, and various arguments obfuscate the actual patentable subject matter that may not have already been identified.

The applicants' arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. Also, in

response to the applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

a) The applicants argue that Imamiya shows a "potential converter" and reveals that it upconverts a clock signal to a higher voltage, therefore it is not a charge pump. However, one of ordinary skill in the art would recognize this upconverter is one type of a charge pump since it utilizes the clock signal to alternately charge and discharge a capacitor, wherein the final output voltage is boosted up (e.g. pumped up) to its desired voltage level when a high voltage out is provided. Since the applicants' admit Imamiya's circuit provides a higher voltage, and that Fig. 10 is one type of a charge pump, Figs. 15A and 15B (which both closely correspond to the circuitry shown in Fig. 10) both show examples of charge pump type circuitry. For example, elements QN11-QN12,QP11-QP12, and C2 of Fig. 15A correspond to Fig. 10's elements QN71-QN72, QP71-QP72, and C71, respectively. Therefore, if the applicants admit Fig. 10 is one type of a charge pump, why wouldn't Fig. 15A also be considered a charge pump? Fig. 15A is identified as converter 5 that corresponds to converters 5 shown in Fig. 14. These converters provide a converted (e.g. pumped) voltage to coupling capacitors C1 when OUT is high. The single-phase charge pump clock output Ø of Fig. 15A is passively coupled to the gates of the switching devices passively since there are no intervening elements, and a connecting line is one type of passive coupling (e.g. as disclosed by Pfiffner). With the

clock output Ø applied to the gates (i.e. control nodes), there will be no substantial transfer current to the control nodes.

b) As for the examiner's use of Pfiffner, it was not cited "for obscure reasons" as the applicants cite on page19 of the amendment. This reference is used as an example that discloses connecting lines as one type of passive coupling, since the applicants have a penchant to argue and question every little thing. Therefore, one of ordinary skill in the art would understand from this reference that one type of passive coupling does not require a distinct capacitor, resistor, inductor, or any other type of a passive device.

c) Yamashiro was cited as one known example of the use of capacitive coupling for providing a single signal to the gate of a corresponding FET. For example, this reference clearly shows a single control signal being used to control two separate switching devices (e.g. transistors), wherein each device receives the control signal through the device's own corresponding capacitor. Therefore, the reference of Yamashiro provides a teaching for coupling a single signal to more than one switching device, thus helping to block undesirable signals (e.g. noise) and minimizing false triggering.

d) Although Ito's reference does not specifically relate the clock generating circuit/ring oscillator to a charge pump circuit, one of ordinary skill in the art would understand Ito's circuit can be used as a clock generating circuit when stable, periodic signals are required. Since charge pump circuits require a clock type signal to control their pumping operations, and numerous references show and disclose the use of ring oscillators used to provide the signals to a charge pump circuit, it would be obvious to

one of ordinary skill in the art to use Ito's circuit/oscillator (or other ring oscillators) as one type of clock generating circuit/ring oscillator required by a charge pump. If ring oscillators are not suitable for charge pumps as the applicants imply on page 24, why do various references of record (e.g. Yamauchi; Forbes et al.; Tasdighi; Fujioka; Gorecki et al.; Kersh, III; Chern, and Itoh) either show or disclose the use of ring oscillators for charge pumps, wherein some of these include ring oscillators with only three stages, and/ or current limiting? From this examiner's perspective, if a charge pump requires at least one control signal from some type of a clock generating circuit, there is no reason a ring oscillator cannot be used to provide that control signal. Also, if the clock generating circuit of a charge pump is critical, why do so many prior art references of record show no control signals being applied to a charge pump; show only lines representing control signals with nothing providing those signals; or generic blocks (e.g. identified as a clock generating circuit, an oscillator, or a ring oscillator) that provides the signal(s). Therefore, this lack of disclosure suggests it is well known to those of ordinary skill in the art that numerous types of circuits can provide the control signal(s). For example, even the applicants disclose "Any clock generator may be employed" in paragraph 070 of the original disclosure. Isn't this an admittance by the applicants that numerous types of circuitry can be used to supply the control signal(s) to the charge pump? Therefore, why wouldn't the examiner's obvious use of Ito's or Yamauchi's ring oscillator be obvious to one of ordinary skill in the art? For the various reasons previously described, there is plenty of motivation to utilize the ring oscillators as described in the formal rejections.

e) Page 21 of the amendment cites Clark does not teach the use of a plurality of discharging switches to a charge pump circuit, but provides high-voltage control voltage for switches. Clark discloses a flying capacitor, and buck-boost circuitry, that one of ordinary skill in the art would recognize as being related to charge pump circuitry. Fig. 1 shows switches 34, 36, 40, and 42 as generic type single switches. However, Fig. 2 shows each one of these single switches as two series coupled switches. Therefore, Clark's invention is related to a charge pump, and the reference clearly shows the use of series coupled switches coupled between a transfer capacitor (i.e. flying capacitor) and either an input to charge the capacitor, or an output receiving the boosted voltage transferred from the capacitor. As such, Clark's reference is an appropriate example of using two series connected switches in place of a single switch. [Incidentally, it is noted that the applicants' own figures fail to show any circuitry with series coupled switches between the transfer capacitor and either the voltage source or the output. Therefore, if the use of series coupled switches is not obvious with respect to Clark's reference, shouldn't series coupled switches be clearly shown at least in the present application, or is this obvious to the applicants and no one else?]

f) It is not understood why the applicants argue the simultaneous conduction of Tasdighi's FET 27 of SW1 and FET 26 of SW2 will probably fail. The applicants cite on page 22 that Tasdighi is not concerned with details of a single phase charge pump passively coupled to FET switches, and "In the absence of such disclosure, Tasdighi cannot serve as evidence that this requirement is known in the prior art." However, this examiner strongly believes such details are left out because these types of operations, and

related obvious type modifications, are well known and understood to one of ordinary skill in the art. Therefore, they do not have to be described in detail. It appears the applicants also have minimal descriptions, wherein various claimed limitations aren't even shown in the figures. If these various items are so critical and important to the claimed invention, why is the present application so minimal with respect to the number of stages within a ring oscillator (e.g. only a three stage ring oscillator is shown and there is nothing in the original disclosure that the ring oscillator can have a single stage, or even have more than one stage); what is considered "substantially sine-like"; where are the series coupled switches shown; etc.)? Although Tasdighi refers to the reference of Bingham, this does not prevent one of ordinary skill in the art from making obvious type modifications (e.g. use of one single-phase signal versus two phase). Which type of signal is used will depend on the conductivity type of each switch, and/or the specific configuration of the switches. For example, if all the individual switches (one pair of individual switches) within each of switches SW1 and SW2 are of the same type, it would be understood two phases would be normally required to ensure only the two individual switches related to charging the capacitor are on at the same time, while the two other individual switches related to transferring the charge to the output are off at the same time, and vice versa. Given the configuration as previously described by the examiner (e.g. each CMOS switch of Tasdighi's Fig. 3 receives the same signal, wherein the transistors within each CMOS switch will have complementary operation), one of ordinary skill in the art would understand that one set of like conductivity transistors (e.g. PMOS) will be turned on to charge capacitor C1 while the other set of the opposite like

conductivity transistors (e.g. NMOS) will be turned off to isolate the capacitor from the output. When the control signal transitions in the opposite direction, the one set of conductivity transistors will be turned off, and the other set of the opposite like conductivity transistors will be turned on to transfer charge to Vout.

g) Page 25 of the amendment refers back to the reference of Hara teaching that ring oscillators for charge pumps should have at least five stages. However, this does not prevent a charge pump's ring oscillator from having three stages since three stage ring oscillators are well known, wherein fewer stages decreases the number of components used, therefore requiring less area and energy consumption. As such, why can't three stage ring oscillator be used when a charge pump can be controlled by a ring oscillator? Also, this is a single reference. Do the applicants have any reference that clearly shows and discloses that ring oscillators controlling charge pumps must have at least five stages? The examiner has provided numerous references that show/disclose ring oscillators can have three stages. Therefore, should these references be completely ignored just because the single reference by Hara cites "should have at least five stages"? This may be convenient to the applicants, but is not reasonable with respect to the broadest interpretation and knowledge of one of ordinary skill in the art. With respect to sine-like related limitations of ring oscillators, previous comments by the applicants imply ring oscillators having fewer stages have more sine-like signals than ring oscillator having more stages. With this type of reasoning, wouldn't a five stage ring oscillator have more sine-like signals than a seven stage ring oscillator? However, related to this, the original disclosure never clearly indicates what makes the signal sine-like. For

example, is it because the ring oscillator has only three stages; stages that have current limiting; and/or a corresponding capacitor coupled between the output of each stage and ground? Therefore, it is suggested the applicants reconsider their own application with respect to what is clearly shown and disclosed.

h) Page 26 of the amendment cites Forbes does not suggest any detail or circuitry for what provides the charge pump clocks. Similar to the reasoning previously described above with respect to Tasdighi et al., it is strongly believed such details are left out because these types of operations, and related obvious type modifications, are well known and understood to one of ordinary skill in the art. Therefore, they do not have to be described in detail. However, Forbes does clearly show switching devices 478 and 482 of Fig. 6, and also switching devices 489 and 491 of Fig. 8, each controlled by a single phase signal. This is because the switching devices are of opposite conductivity types, and a single signal will allow one device to be off while the other is on to ensure the charging/charge transferring operations are performed correctly. As previously described, one of ordinary skill in the art understands some type of circuitry is needed to supply the control signal, and a ring oscillator is one known means of doing that. As previously described, such a ring oscillator can have three stages, and/or can have current limiting.

i) The applicants admit Yamauchi uses a current-starved ring oscillator as a charge pump clock, and ring oscillators have an odd number of stages. However, the applicants then indicate that Yamauchi's Figs. 6 & 7 suggest more than three stages due to the use of "..." within the figures, and because of the lack of any suggestion by

Yamauchi that a three stage ring oscillator is possible. Again it appears the applicants are using an extremely narrow interpretation of the prior art, ignoring what those of ordinary skill in the art would understand. However, the examiner utilizes the broadest reasonable interpretation of the claimed limitations and prior art references. If the examiner applied the applicants' same type of narrow interpretive reasoning to the applicants' own ring oscillator, the applicants can only claim a ring oscillator with three stages since that is all that is clearly shown and described in the original disclosure. However, one of ordinary skill in the art would reasonably understand that Yamauchi's ring oscillator can also have three stages. For example, if three stages, an odd number, will provide a sufficient output signal, why would more stages be used? A three stage ring oscillator utilizes fewer components, thus using less overall area and energy.

Prior Art

The prior art references cited on the accompanying PTO-892 are deemed relevant to at least sections of the claimed invention, since they show or disclose what is already well-known to one of ordinary skill in the art. Tsukada shows another example of a charge pump being controlled by a current-starved type ring oscillator in Figs. 1 and 4. Kurafuji's Fig. 1 shows what can be considered one type of single stage ring oscillator OSC providing a signal to a charge pump comprising Cc,D1-D2, and Fig. 3 shows OSC as a ring oscillator having three stages. [Note: Whether the OSC is considered a single stage ring oscillator (e.g. see Fig. 1) or a three stage ring oscillator (e.g. see Fig. 3), its output in Fig. 1 is shown as a square wave. Therefore, it appears that even a one (or three) stage ring oscillator does not necessarily provide a sine-like output as the applicants have previously implied. As such, must the current limiting devices

508-518 and capacitors 520,522 within the applicants' Fig. 5 ring oscillator 500 be present to ensure CLK 524 is "substantially sine-like"?] Fig. 3A of Yoshida et al. shows a charge pump comprising switching devices 22-25 without clearly showing what controls them; and Fig. 9A shows two series connected switching devices while Fig. 9B shows a single switching device. Thurber, Jr. shows charge pump S1-S2,C-x in Fig. 5 being controlled by a single (phase) output from OSC, wherein Fig. 6 shows OSC providing two separate (phase) outputs controlling the switches. Although Thurber, Jr. does not clearly identify OSC as a ring oscillator, the reference does disclose OSC (of Fig. 3) as "free-running", which one of ordinary skill in the art would recognize as being one type of a ring oscillator. Figs. 18 and 19 of Utsunomiya et al. each show a booster circuit (e.g. one type of a charge pump), wherein the switching devices of Fig. 18 are controlled by a two-phase signal (i.e. 224 and 225), and the switching devices of Fig. 19 are all controlled by a single-phase signal (i.e. 245) because the conductivity type of one transistor (see NMOS 227 of Fig. 18 versus PMOS 247 in Fig. 19) was changed. Therefore, all of these references show or disclose various known circuitry and modifications one of ordinary skill would be familiar with. As such, each reference provides its own corresponding motivation(s) to make obvious type modifications (to other known circuitry) similar to the various reasoning provided by the examiner in the various formal rejections described above. For example, if a charge pump is controlled by two phases, a change to the conductivity type of one (or more) switching devices can be made to allow the charge pump to be controlled by a single phase as shown by Utsunomiya et al. Of course, one of ordinary skill in the art would also understand that some type of circuitry must be provided to provide the phase(s).

For the numerous reasons described above, the rejections described in this Office Action are deemed proper with respect to the broadest reasonable interpretation of the claimed limitations and of the prior art of record.

THIS ACTION IS MADE FINAL. The applicants are reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, N. Drew Richards, can be reached on (571) 272-1736.

The new central official fax number is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE

Terry L. Englund

15 November 2007

N. DREW RICHARDS
SUPERVISORY PATENT EXAMINER